REMARKS

Claims 8 and 9 have been canceled. Claims 1-7, 11-14, and amended claims 10 and 15 are in this application.

Claims 1-7 were rejected under 35 U.S.C. 103(a) as being unpatentable over JP 02249333 (Hirade, Junji et al.) in view of U.S. Patent No. 4,713,605 A (Iyer et al.).

Independent claim 1 recites in part the following:

> "**switching means supplied with the scramble-processed data and the bit data of the predetermined pattern** generated by the data generating means to select the bit data of the predetermined pattern at the time of synchronization processing of transmit data, and to select the scramble-processed data when synchronization processing of transmit data is not performed to output the data thus selected as scrambler output data,
>
> **the generated bit data** of the predetermined pattern **supplied to the one or more of the shift registers is the same as the generated bit data of the predetermined pattern supplied to the switching means**." (Emphasis added.)

In explaining the 103 rejection with regard to claim 1, the Examiner appears to assert that the switching circuit 2 of Hirade is the same as the switching means of claim 1; and the Examiner appears to assert that Fig. 2, lines 23-29 and 42-47 of column 4, and the Abstract of Iyer teach "the generated bit data . . . supplied to the one or more of the shift registers is the same as the generated bit data . . . supplied to the switching means" of claim 1 wherein element 130 of such Fig. 2 is the switching means of claim 1.

Initially, it is noted that the Examiner appears to rely on two different elements for the switching means of claim 1----that is, switching circuit 2 of Hirade and element (or

switch) 130 of Fig. 2 of Iyer. It is respectfully submitted that neither the switching circuit 2 of Hirade nor the switch 130 of Iyer appears to be the same as the switching means specifically recited in claim 1. More specifically, the switching means of claim 1 may be supplied with (i) scramble-processed data and (ii) the bit data of the predetermined pattern generated by the data generating means; and the switching means of claim 1 may select the bit data of the predetermined pattern at the time of synchronization processing of transmit data and the scramble-processed data when synchronization processing of transmit data is not performed. As an example thereof, reference is made to Fig. 4 of the present application. With regard to Hirade, the switching circuit 2 of Hirade does not appear to be supplied with scramble-processed data and does not appear to select the scramble-processed data when synchronization processing of transmit data is not performed. With regard to Iyer, the switch 130 of Iyer also does not appear to be supplied with scramble-processed data and, as such, does not appear to select the scramble-processed data when synchronization processing of transmit data is not performed.

Thus, since neither Hirade nor Iyer as applied by the Examiner appears to disclose the switching means specifically recited in claim 1, it is respectfully submitted that claim 1 is distinguishable from the applied combination of Hirade and Iyers.

Accordingly, it is respectfully requested that the above 103 rejection of claim 1 be withdrawn.

For reasons similar to or somewhat similar to those previously described with regard to claim 1, it is also respectfully requested that the above 103 rejection of independent claim 5 be withdrawn.

Claims 2-4, 6, and 7 are dependent from one of independent claims 1 and 5. Accordingly, it is also respectfully requested that the above 103 rejection of claims 2-4, 6, and 7 be withdrawn for at least the reasons previously described.

Claims 10-14[1] were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,535,239 A (Padovani et al.) in view of U.S. Patent No. 4,827,514 A (Ziolko et al.).

Amended independent claim 10 now recites in part the following:

> "a random number generating circuit to generate a random bit data train, **said random number generating circuit having a first shift register, a second shift register, and a first adder**, said random number generating circuit being arranged such that (i) an output stage of the first shift register is coupled to an input stage of the second shift register and to the first adder **such that during operation an output from the first shift register is supplied to the input stage of the second shift register and to an input of the first adder**, and (ii) an output stage of the second shift register is coupled to the first adder **such that during operation an output of the second shift register is supplied to another input of the first adder**;" (Emphasis added.)

In explaining the 103 rejection with regard to claim 10, the Examiner appears to assert that elements 62, 64, and 66 of Fig. 3 of Padovani are the same as the random number generating circuit of claim 10. In response, it is respectfully submitted that elements 62, 64, and 66 of Fig. 3 of Padovani are not the same as the random number generating circuit as now

[1] Although the Examiner only indicated that claims 10-14 were rejected in line 1 of section 3 of the present Office Action, it is believed that the Examiner intended to reject claims 10-15 herein.

specifically recited in claim 10. As an example, such elements of Padovani do not appear to be the same as "a random number generating circuit . . . [which has] a first shift register, a second shift register, and a first adder . . . arranged such that . . . during operation an output from the first shift register is supplied to the input stage of the second shift register and to an input of the first adder, and . . . such that during operation an output of the second shift register is supplied to another input of the first adder," as now recited in claim 10.

Accordingly, it is respectfully submitted that the applied combination of Padovani and Ziolko does not appear to disclose all of the above-identified features now recited in claim 10.

Thus, it is respectfully requested that the above 103 rejection of claim 10 be withdrawn.

For reasons similar to or somewhat similar to those previously described with regard to claim 10, it is also respectfully submitted that amended independent claim 15 is also distinguishable from the applied combination of Padovani and Ziolko. As such, it is also respectfully requested that the above 103 rejection of claim 15 be withdrawn.

Claims 11-14 are dependent from independent claim 10. Accordingly, it is also respectfully requested that the above 103 rejection of claims 11-14 be withdrawn for at least the reasons previously described.

As it is believed that all of the rejections set forth in the Official Action have been overcome, favorable reconsideration and allowance are earnestly solicited. If, however, for any reason the Examiner does not believe that such action can be taken at this time, it is respectfully requested

that the Examiner telephone applicant's attorney at (908) 654-5000 in order to overcome any additional rejections and/or objections which the Examiner might have.

If there are any charges in connection with this requested amendment, the Examiner is authorized to charge Deposit Account No. 12-1095 therefor.

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Respectfully submitted,

By _____

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